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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Elve Desiderius Jozef MOONS, et al.

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For: OPERATIONAL AMPLIFIER ARRANGEMENT

SUBMISSION OF PRIORITY DOCUMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is a certified copy of the priority document on which a claim to priority was made under 35 U.S.C. § 119. The Examiner is respectfully requested to acknowledge receipt of said priority document.

Respectfully submitted,

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

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23373
CUSTOMER NUMBER

David J. Cushing
Registration No. 28,703

Enclosures: Europe 02292307.2

Date: January 7, 2004

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Bescheinigung | Certificate | Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

02292307.2

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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R C van Dijk

Anmeldung Nr:
Application no.: 02292307.2
Demande no:

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Anmelder/Applicant(s)/Demandeur(s):

ALCATEL
54, rue la Boétie
75008 Paris
FRANCE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Operational amplifier arrangement

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OPERATIONAL AMPLIFIER ARRANGEMENT

The present invention relates to an operational amplifier arrangement, and more particularly operational amplifier arrangements which can be used as line drivers in telecommunication line circuits.

Line driver circuits are already known in the art and comprise the classical class-G-based operational amplifiers such as these for instance described in published European Patent Applications 1 024 592 and 1 024 591. Other line driver circuits are based on switching line drivers such as the one described in the published European Patent Application 1 229 641. Yet other types of line drivers are based on class C-AB architectures, such as these disclosed in published European Patent application 1 220 442 and 1 220 443. Key issues for line drivers in applications such as ADSL , which is the abbreviation of asymmetric digital subscriber line, are the power efficiency, the linearity and the complexity. Although all types of abovementioned line drivers were conceived such as to optimize these issues, yet there remains a need for improvement of the power efficiency, and linearity, while at the same time keeping the complexity of the operational arrangement as low as possible. This is especially important for very high speed digital subscriber line applications, hereafter abbreviated with VDSL.

An object of the present invention is thus to provide an operational amplifier arrangement which is power efficient, linear and simple.

According to the invention, this object is achieved due to the fact that said operational amplifier arrangement further includes the features as described in claim 1.

In this way, a new operational amplifier arrangement architecture is provided having a very good linearity, which is simple and which is very power efficient. Its operation will be described into detail in the descriptive part of this document, but can be summarized briefly by stating that the non-linear amplifier drives maximum power to the line with a maximum efficiency, whereby the linear amplifier is correcting the non-linearities caused by this non-linear amplifier, such as cross-over errors, slew rate and other distortions.

A further characteristic feature of the present invention is described in claim 2.

Thereby power efficiency is further improved by the fact that said non-linear amplifier is working at a reduced supply voltage, such that it is clipping on the high input signal levels. However these additional errors are further corrected by means of the linear amplifier which is operative at the highest supply voltage level, and which can thus correct these clipping errors.

Further characteristic features of the present invention are shown in claims 3 to 7.

Thereby differential embodiments are provided, for driving differential signals to two-wire loads. The relationships between corresponding amplifiers, resistors and active back terminating arrangements thereby guarantees further linearity and symmetry of the differential embodiments.

Additional characteristic feature of the present invention ar mentioned in claims 8 and 9.

This further improves the power efficiency of the differential embodiment by means of a more pronounced application of the so-called "active back termination" principle. The active back termination principle is thereby exploited to another resistor level, thereby further improving the power efficiency while still keeping the same low complexity and good linearity.

Yet other characteristic features of the present invention are stated in claim 10 and 11.

These define additional requirements for operation of the operational amplifier arrangements , which further enables selecting appropriate resistors and amplifiers .

Another characteristic features of the present invention are described in claims 12 and 13.

These conditions present further restrictions for the resistors in the different embodiments claimed in case these operational amplifiers need to terminate a series load impedance, such as is the case for a line driver application.

It is to be noticed that the term 'coupled', used in the claims, should not be interpreted as being limitative to direct connections only. Thus, the scope of the expression 'a device A coupled to a device B' should not be limited to devices or systems wherein an output of device A is directly connected to an input of device B. It means that there exists a path between an output of A and an input of B which may be a path including other devices or means.

It is to be noticed that the term 'comprising', used in the claims, should not be interpreted as being limitative to the means listed thereafter. Thus, the scope of the expression 'a device comprising means A and B' should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

The above and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wherein

Figure 1 gives a schematic of a single-ended embodiment of an operational amplifier arrangement OAA according to the invention,

Figure 2 schematically depicts a first differential embodiment of an operational amplifier arrangement according to the invention,

Figure 3 depicts another differential embodiment of an operational amplifier arrangement according to the invention,

Figure 4 depicts a third differential embodiment of an operational amplifier arrangement according to the invention,

Figure 5 depicts a fourth differential embodiment of an operational amplifier arrangement according to the invention, and

Figure 6 gives an equivalent schematic, depicting the principal operation of the embodiment of Fig. 1 and the embodiments of Figs 2 to 4, according to the invention.

The operational amplifier arrangement OAA depicted in Fig. 1 includes an input terminal IN, an output terminal OUT, and two pairs of supply terminals (not shown on Fig. 1). To this single-ended embodiment is provided an input voltage from a source Vin, for instance being the signal delivered by the D-A converter in ADSL applications. This input terminal is coupled to the respective input terminals of two amplifiers : a non-linear amplifier A2 and a linear amplifier A3. Such a non-linear amplifier may for instance consist of a class-B amplifier as indicated in Fig. 1. However, other types of non-linear amplifiers are possible such as switching mode amplifiers , class C or class D amplifiers. In general a very power efficient amplifier will be chosen for this non-linear amplifier in this operational amplifier arrangement. For the linear amplifier A3, class A or AB amplifiers can be used . In a preferred embodiment, the non-linear amplifier power supply terminals are coupled to one pair of supply terminals of the operational amplifier arrangement, whereas the linear amplifier has power supply terminals which are coupled to the other pair of supply terminals of the operational amplifier arrangement. The supply voltage of the linear amplifier is thereby higher in amplitude than the supply voltage of the non-linear amplifier. A consequence of this is that high input signals will be clipping to the lower supply voltage levels of the non-linear amplifier, whereas these can yet be amplified nicely by the linear amplifier operating between supply rails of a higher voltage. However in other embodiments both linear and non-linear amplifiers are operative between the highest supply voltage. Power efficiency of the arrangement is nevertheless improved for the preferred embodiment whereby the non-linear amplifier operates at a lower supply voltage than the linear amplifier.

The non-linear amplifier A2 has an output terminal OUT A2, and has a first feedback impedance RFA2 coupled between this output terminal OUTA2 and an input terminal IN1A2. Another input terminal IN2A2 of this amplifier is coupled to the ground reference in this single-ended embodiment. The input voltage may be reduced by means of an input resistor RinA2 coupled between the input terminal IN of the arrangement and the first terminal IN1A2.

Similarly, another input resistor RINA3 may be placed in the input path of the linear amplifier A3 , thus between the arrangement input terminal IN and a first input terminal IN1A3 of the linear amplifier A3. This linear amplifier similarly has a second input terminal IN2A3, coupled to the ground reference. The output terminal OUTA3 of the linear amplifier is further coupled via a second feedback impedance RFA3, to the first input terminal IN1A3, and also to the output terminal OUTA2 of the non-linear amplifier, by means of an output series impedance R1. OUTA3 is also coupled to the arrangement output terminal OUT, via a terminating impedance Rterm.

The operational amplifier arrangement OAA further includes an active backterminaton arrangement, which, in the embodiment depicted in Fig. 1 simply consists of a feedforward impedance RFABT, coupled between the arrangement output terminal OUT and the second input terminal IN2A3. In another embodiment this active back termination arrangement may consist of an invertor in series with a similar feedforward impedance, both of which are coupled in series between the arrangement output terminal OUT and the first input terminal IN1A3 of the linear amplifier A3.

This feedforward coupling realised by the active backterminaton arrangement is crucial in the operation of the amplifier arrangement OAA since in this way distorted signals coming from the non-linear amplifier A2, are thereby fed back to an input of the linear amplifier A3 . This linear amplifier thereby amplifies them , but due to the inversion operation of the active back termination also subtracts them from the total signal as appearing on the summing nodes OUTA3 and OUT. The distorted signal from the non-linear amplifier is thus again corrected by means of the linear amplifier.

It is thereby also mandatory that the gain which is provided by the non-linear amplifier part between IN and OUT , thus including RINA2, A2, RFA2, R1 and Rterm equals the gain which is provided by the linear amplifier part between IN and OUT, including RINA3, A3, RFA3, RjA3, RFABT and RTERM. Furthermore, it is also mandatory that the part of the output impedance of the arrangement, seen from the output terminal , with only RTERM, A3, RFA3, RFABT

concerned, has to be the same as the part of the output impedance of the arrangement, also seen from the output terminal , but with only RTERM, R1, A2 and RFA2 concerned. The philosophy behind both requirements is that the operational amplifier arrangement consists of two equivalent paths in parallel of which the possible distortions caused by the non-linear amplifier are corrected by means of the linear one.

The principle of operation of the active back termination arrangement of this embodiment is made clear by means of the equivalent scheme which is depicted in Fig. 6. Following equations hold :

$$Zline = R1 + Rterm \qquad (1),$$

since Zline which, in Fig. 6 and in Fig. 1, corresponds to the load impedance, has to be equal to the output impedance Zout for appropriately terminating the amplifier arrangement to the line impedance as is mandatory in order to avoid reflections.

Furthermore,

$$VoutA3 = (Vin - (Zout/G).Iout.G).A3 \qquad (2)$$

whereby G is the gain of the block consisting of amplifier A1, and impedances k.Rterm, and k.Zline, depicted by means of their resistance values, and A3 here depicts the gain of the linear amplifier A3 and its input resistors and feedback resistors.

Since Zout/G equals Rterm, this equation means that the voltage across Rterm, being Iout.Rterm, multiplied by the gain of the block G appears at the input of A3, whereby it is subtracted from the input Vin.

Equation (2) can be further reduced to :

$$VoutA3 = (Vin - IoutxZout)A3 \qquad (3)$$

By means of the presence of amplifier A5

$$Vout = VoutA3 \quad (4)$$

Such that

$$Vout = (Vin - IoutxZout)A3 \quad (5)$$

Equation (5) thus gives the basis for the synthesis of Zout, which needs to be equal to the load impedance, corresponding to the line impedance Zline, in the case of a line driver. This is performed by the Active back termination arrangement, which, in a very simple embodiment can merely consist of one resistor coupled between the arrangement output terminal and an input terminal of the linear amplifier, as was already described for the embodiment of Fig. 1.

Remark that in the scheme depicted in Fig. 6 all amplifiers are inverting amplifiers. This is the reason why an additional inversion, denoted by A4, is to be further included such as to obtain the correct equations. Remark also that the added resistor RinA3 was needed such as to accomplish the summing operation, whereby in the equivalent scheme of Fig. 6 the positive input is kept to the ground reference since the feedback from the output was feeded to the same input terminal to which the input signal was supplied. In the scheme of Fig. 1 the feedback from the output signal on the output terminal OUT was fed to the other input terminal of A3. The presence of amplifier A5 in this equivalent scheme thereby forces the voltage VoutA3 to be equal to the output voltage Vout.

Other embodiments of an operational amplifier according to the invention are depicted in Figs. 2 to 5. In Fig. 2 a differential embodiment OAA', including two halfs, each of which is similar to the embodiment depicted in Fig. 1, is shown. The first half, coupled to input terminal IN, includes a non-linear amplifier A2, possibly operating at a lower supply voltage than a linear amplifier A3. The linear amplifier has input resistors RinA3, RiA3, and a feedback resistor RFA3, whereas the non-linear amplifier A2 of the first branch includes has input resistor RinA2, feedback resistor RFA2. The output terminal OUTA2 of the non-

linear amplifier A2 is coupled via a series impedance R1 to the output terminal OUTA3 of the linear amplifier A3. A terminating impedance Rterm is coupled between OUTA3 and a first arrangement output terminal OUT, whereby this first arrangement output terminal is coupled via an active backtermination arrangement, in the embodiment depicted in Fig. 2 simply consisting of a resistor RFABT , is coupled to an input terminal IN2A3 of the linear amplifier A3.

Similarly, the other half , with input terminal IN' ,includes as well a linear amplifier A3' and a non-linear amplifier A2'. Linear amplifier A3' has input resistors RinA3' and RjA3', and a feedback resistance RFA3'. Non-linear amplifier A2' has input resistor RinA2', and feedback resistor RFA2'. The single output of A2', denoted OUTA2' is coupled via a second series impedance R1' to the output terminal OUTA3' of A3'. A second terminating impedance Rterm' is coupled between OUTA3' and the second arrangement output terminal OUT', whereas this second arrangement output terminal is coupled to an input terminal of the linear amplifier A3' via a second active backtermination arrangment ABT', in the embodiment depicted in Fig. 2 simply consisting of an impedance RFABT' coupled between OUT' and IN2A3' .

For stability, symmetry and linearity reasons both halfs are realised using substantially equal devices. Thus A2 and A2' are chosen as similar amplifiers, as well as A3 and A3' whereby also the respective input and feedback impedances of the corresponding amplifiers have substantially equal values. Series impedances R1 and R1' are similar as well as, terminating impedances Rterm and Rterm' and active backterminating impedances RFABT and RFABT'.

Because of the differentiality, the load impedances in both halfs may also be halved with respect to the load impedance in the single ended embodiment. This is the reason why these are depicted by a load impedance denoted Zline/2 in Fig. 2

The differential operational amplifier arrangement "OAA" depicted in Fig. 3 also includes two arrangement input terminals IN1" and IN2", as well as two arrangement output terminals OUT1" and OUT2", but only includes one amplifier of each type, namely a linear amplifier A3", again operating between

the highest supply voltage rails, and a non-linear amplifier A2" possibly operating at a lower supply voltage.

Both linear and non-linear amplifiers have two input terminals and two output terminals, respectively coupled to the two arrangement input terminals and the two arrangement output terminals as can be observed from Fig. 3. The arrangement input terminals are thereby coupled to the linear amplifier input terminals via two respective input resistors, both denoted RinA3" which are also substantially equal because of stability. Similarly two substantially equal input resistors, both denoted RinA2" are coupled between arrangement input terminals and respective non-linear amplifier input terminals. A3" has two similar feedback impedances, both denoted RFA3". The same holds for A2" having also two similar feedback impedances both denoted RFA2" becaus they have substantially equal values. Output terminals of A2" are coupled to corresponding output terminals of A3" via respective series impedances, both denoted R1" because they are similar . With corresponding output terminals is meant that both output terminals of these amplifiers are delivering the same sign of signal at a moment in time. In other words, the positive output terminal of A2" is coupled to the positive output terminal of A3" and vice versa.

The output terminals of A3" are further coupled to the corresponding arrangement output terminals OUT1" and OUT2" via respective terminating impedances , both denoted Rterm" since these are also similar for symmetry reasons. In the embodiment depicted in Fig. 3, these arrangement output terminals are coupled to the non-corresponding input terminals of the linear amplifiers via respective active back terminating arrangements, in the embodiment depicted in Fig. 3 merely consisting of resistors. In other embodiments however these active back terminating arrangements may again consist of a series coupling of a resistor and an invertor, in which case arrangement output terminals are connected via this type of active back terminating arrangements, to the corresponding input terminals of the linear amplifier A3".

Yet another differential embodiment, OAA10 which shows a lot of resemblance with the one depicted in Fig. 2, is shown in Fig. 4. It again consists of two halfs : a first one consisting of a first parallel branch including non-linear amplifier A20, series impedance R10 and terminating impedance Rterm10, and a second parallel branch with linear amplifier A30 and the same terminating impedance Rterm10. Both amplifiers may further have feedback such as depicted by RFA20 and RFA30 respectively, as well as input resistance respectively depicted by RinA20 and RinA30.

The second half of the embodiment of Fig. 4 again consists of two parallel branches : a first one via linear amplifier A31 and a second terminating impedance denoted Rterm11, and a second one via non-linear amplifier A21, series impedance R11 and terminating impedance Rterm11. As in the first half, the respective amplifiers may have respective input resistors , respectively denoted RinA31 and RinA21, as well as feedback, respectively denoted by RFA31 and RFA21.

The difference with respect to the embodiment depicted in Fig. 2 lies in the coupling of the active back termination arrangements between the arrangment output terminals and the input terminals of the linear amplifiers . As can be easily observed by comparing both figures, active back terminating resistor RFABT10 is coupled between an arrangement output terminal belonging to one upper half of the arrangement, and an input terminal of the linear amplifier belonging to the lower half of the arrangement. Similarly, active back terminating resistor RFABT11 is coupled between an arrangement output terminal of the lower half to an input terminal of the linear amplifier of the upper half. This embodiment merely presents an alternative embodiment for realising the active back termination, as compared to the embodiment of Fig. 2

The embodiment depicted in Fig. 5 is basically similar to the one depicted in Fig. 4, except for the addition of another pair of active backterminating arrangements, in the embodiment of Fig. 5 consisting of resistors RFABT100 and RFABT101 respectively. This second pair of active back terminating resistors is thereby cross-coupled between an output terminal of a

linear amplifier of one half of the arrangement, to an input terminal of a non-linear amplifier of the other half of the arrangement. Thus, in Fig. 5, output terminal of A31' is coupled to input terminal of A20' via active back terminating resistor RFABT101 while output terminal of A30' is coupled to input terminal of A21' via active back terminating resistor RFABT100. The presence of a second pair of active backtermination resistors even improves the power effectiveness of the arrangement since this allows to select the series resistances R10' and R11' to be lower compared to the configuration of Fig. 2 . In this case equivalent scheme of Fig. 6 and according formula's are no longer valid. However the total output impedance of the arrangement OAA10' still needs to be the same to the load impedance .

In Fig. 5 the second active back termination is realised by means of cross-coupling. However in an alternative embodiment the output of the linear amplifier A31 can also be coupled , via a single resistor, to the "+" input of A21' , or via a series connection of a single resistor and an invertor to the "-" input of A21' for the embodiment depicted in Fig. 5. Similar considerations hold for the active back termination in the upper half of the scheme.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention, as defined in the appended claims.

CLAIMS

1. Operational amplifier arrangement (OAA;OAA") including an arrangement input terminal (IN; IN1") to which an input voltage is supplied and an arrangement output terminal (OUT; OUT1") terminal, said operational amplifier arrangement further comprising

- a non-linear amplifier (A2;A2") , having a pair of input terminals one of which is coupled to said arrangement input terminal, said non-linear amplifier further including an output terminal coupled to said arrangement output terminal (OUT;OUT1")
- a linear amplifier (A3) , having a pair of input terminals one of which is coupled to said arrangement input terminal, said linear amplifier further including an output terminal which is coupled to said arrangement output terminal (OUT;OUT1") ,
- whereby the output terminal of said non-linear amplifier (A2;A2") is coupled to the output terminal of said linear amplifier (A3;A3") via a series impedance (R1;R1"),
- whereby the output terminal of said linear amplifier (A3;A3") is coupled to the arrangement output terminal (OUT;OUT1") via a terminating impedance (Rterm;Rterm"),
- and whereby the arrangement further includes an active backtermination arrangement (ABT;RFABT") coupled between the arrangement output terminal (OUT;OUT1") and either one of said pair of input terminals of said linear amplifier (A3;A3").

2. Operational amplifier arrangement (OAA;OAA") according to claim 1

characterised in that

said non-linear amplifier (A2;A2") is operating between a first power supply (VA2) , while said linear amplifier (A3;A3") is operating between a second power supply (VA3) which exceeds the supply voltage of said first power supply source.

3. Operational amplifier arrangement (OAA") according to claim 1 or 2

characterised in that

said operational amplifier arrangement (OAA") further includes a second arrangement input terminal (IN2") , and a second arrangement output terminal (OUT2") terminal, said input signal being a differential input signal, applied between said first arrangement input terminal (IN1") and said second arrangement input terminal (IN2"), between said pair of input terminals of said linear amplifier and applied between said pair of input terminals of said non-linear amplifier, said non-linear amplifier (A2") thereby including a second output terminal coupled to said second arrangement output terminal (OUT2') via a second series impedance (R1"), said linear amplifier (A3") thereby including a second output terminal coupled to the second arrangement output terminal (OUT2') via a second terminating impedance (Rterm"), said operational amplifier arrangement further including a second active backtermination arrangement (ABT") coupled between said second arrangement output terminal (OUT2") and the other one of said pair of input terminals of said linear amplifier (A3").

4. Operational amplifier arrangement (OAA") according to claim 3 characterised in that

said first series impedance (R1") is substantially equal to said second series impedance (R1"), said first terminating impedance (Rterm") is substantially equal to said second terminating impedance (Rterm"), said first active back termination arrangement (RFABT") is substantially equal to said second active back termination arrangement (RFABT").

5. Operational amplifier arrangement (OAA'; OAA10; OAA10') including a pair of arrangement input terminals (IN,IN'; IN10,IN11; IN10',IN11') and a pair of arrangement output terminals (OUT,OUT';

OUT10,OUT11; OUT10',OUT11'), said operational amplifier arrangement further comprising

- first and second non-linear amplifiers (A2,A2'; A20,A21; A20',A21') , coupled between said arrangement input terminals and said arrangement output terminal
- first and second linear amplifiers (A3,A3';A30,A31; A30',A31') , coupled between said arrangement input terminals and said arrangement output terminals,
- whereby respective output terminals of said non-linear amplifiers are coupled to respective output terminals of said linear amplifiers via respective series impedances (R1,R1';R10,R11; R10',R11'),
- whereby respective output terminals of said linear amplifiers are coupled to respective arrangement output terminals via respective terminating impedances (Rterm,Rterm'; Rterm10,Rterm11; Rterm10',Rterm11'),
- and whereby the arrangement further includes a pair of active backtermination arrangements (RFABT,RFABT'; RFABT10,RFABT11; RFABT10',RFABT11') coupled between respective arrangement output terminals and either one of said pair of input terminals of either pair of linear amplifiers (A3,A3'; A30,A31; A30',A31').

6. Operational amplifier arrangement according to claim 5 characterised in that

said first and second non-linear amplifiers (A2,A2'; A20,A21; A20',A21') are operative between a first power supply voltage (VA2) ,

said first and second linear amplifiers (A3,A3';A30,A31; A30',A31') are operative between a second power supply voltage (VA3) which exceeds said first power supply voltage (VA2).

7. Operational amplifier according to claim 5 or 6 characterised in that

said respective series impedances (R1,R1';R10,R11; R10',R11') have substantially equal resistance values, said first and said second non-linear amplifiers (A2,A2'; A20,A21; A20',A21') are substantially identical, said first and said second linear amplifiers (A3,A3';A30,A31; A30',A31')are substantially identical, said respective terminating impedances (Rterm,Rterm'; Rterm10,Rterm11; Rterm10',Rterm11') are substantially identical, said active backtermination arrangements of said pair of active backtermination arrangements (RFABT,RFABT'; RFABT10,RFABT11; RFABT10',RFABT11') are substantially identical.

8. Operational amplifier arrangement (OAA10') according to claim 5, 6 or 7

characterised in that

said operational amplifier arrangement (OAA10') includes a second pair of active back terminating arrangements (RFABT100,RFABT101) coupled between the respective output terminals of said first and said second linear amplifiers and either input terminals of either said first or said second linear amplifiers (A30',A31).

9. Operational amplifier arrangement according to claim 8

characterised in that

the active back terminating arrangements of said second pair of active backterminating arrangements are substantially idential.

10. Amplifier arrangement according to any of the previous claims

characterised in that

the gain of a branch between one of said arrangement input terminals coupled in series with one of said linear amplifiers, said terminating resistance to one of said arrangement output terminals

equals the gain of a parallel branch between said one arrangement input terminal in series with one of said non-linear amplifiers said series

resistance and said terminating resistance to said one of said arrangement output terminals .

11. Amplifier arrangement according to claim 10

characterised in that

the output impedance between one of said arrangement output terminals and one of said arrangement input terminals via said branch equals the output impedance between said one arrangement output terminal and said one arrangement input terminal via said parallel branch .

12. Operational amplifier arrangement according to any of the previous claims 1 to 7

characterised in that

the sum of said respective series impedance and said respective terminating impedance in series with said respective series impedance is equal to the series load impedance .

13. Operational amplifier arrangment according to claim 8 or 9

characterised in that

the sum of said respective series impedance and said respective terminating impedance in series with said respective series impedance is lower than the series load impedance.

ABSTRACT

OPERATIONAL AMPLIFIER ARRANGEMENT

An operational amplifier arrangement is disclosed which comprises a non-linear amplifier and a linear amplifier, both having a pair of input terminals one of which is coupled to an arrangement input terminal, and both having an output terminal which is coupled to an arrangement output terminal , whereby the output terminal of said non-linear amplifier is further coupled to the output terminal of said linear amplifier via a series impedance, whereby the output terminal of said linear amplifier is coupled to the arrangement output terminal via a terminating impedance , and whereby the arrangement further includes an active back termination arrangement coupled between the arrangement output terminal and either one of said pair of input terminals of said linear amplifier. In a preferred embodiment said linear amplifier is operating between a power supply which exceeds the supply voltage of the power supply of said non-linear amplifier. Differential embodiments of this basic configuration are also described.

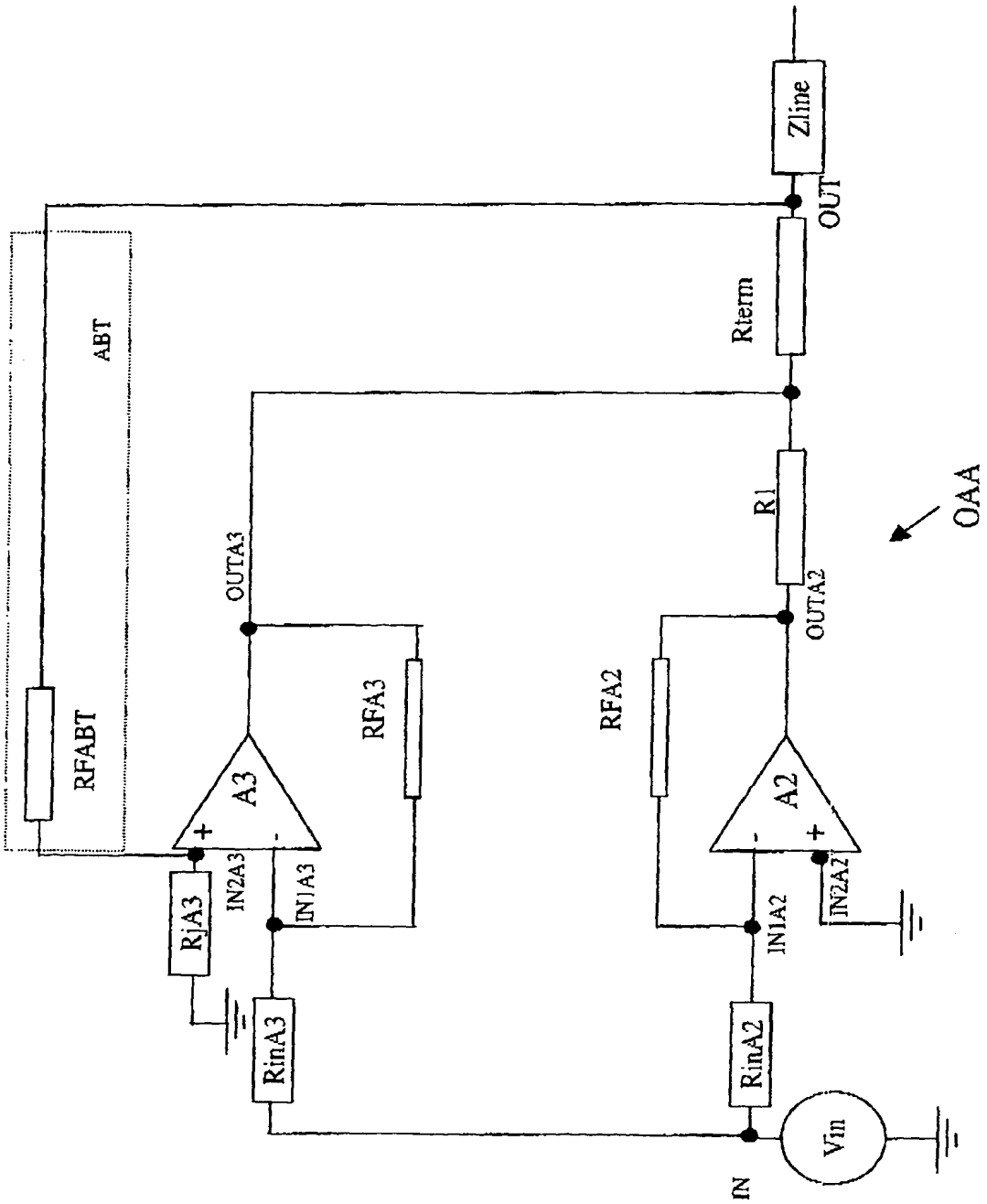
Zline
OUT
Rterm
R1
OAA
OUTA2
OUTA3
ABT
RFABT
RFA3
RFA2
A3
A2
+
-
IN2A3
IN1A3
IN1A2
IN2A2
RjA3
RinA3
RinA2
Vin
IN

Fig. 1

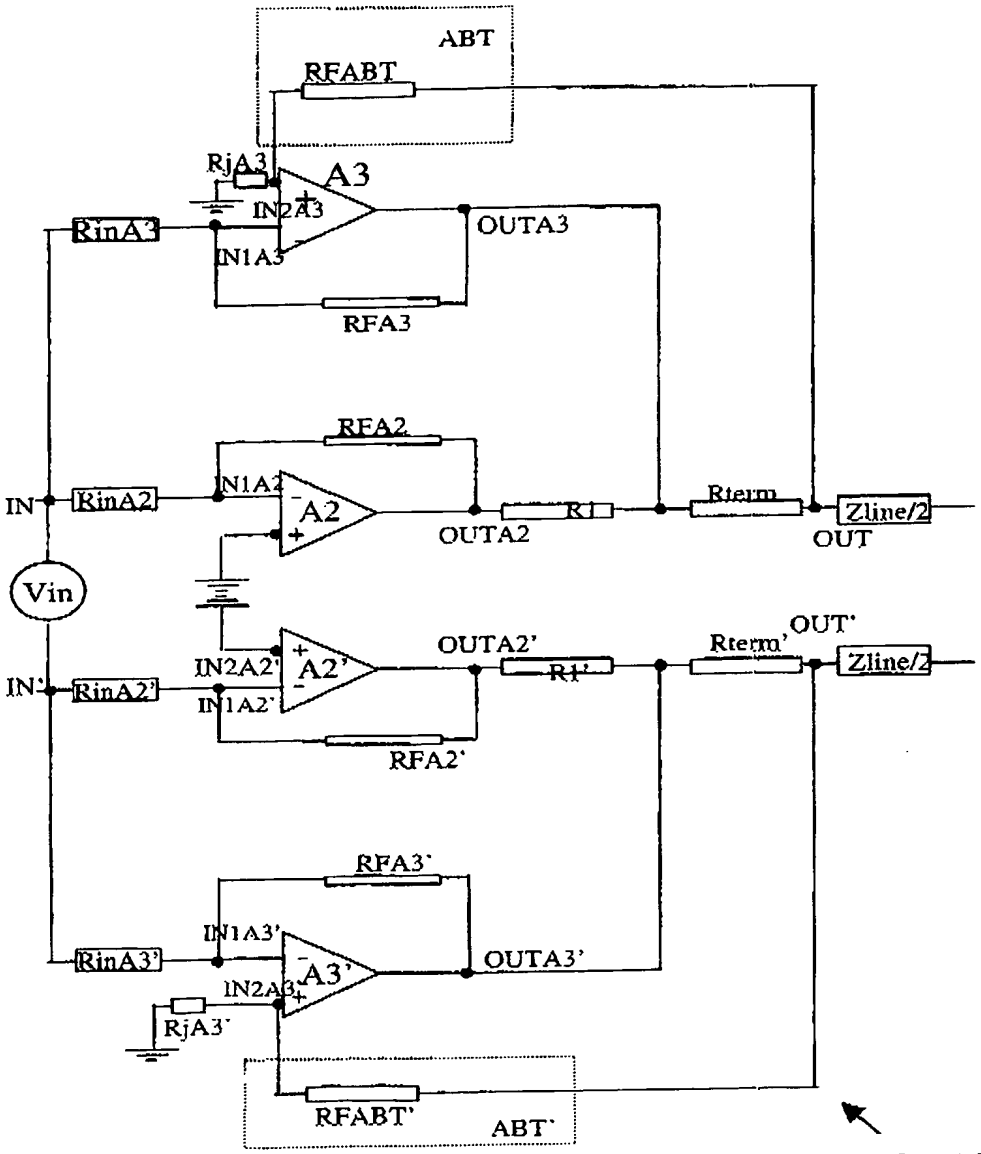
ABT
RFABT
RjA3
A3
IN2A3
RinA3
IN1A3
OUTA3
RFA3
RFA2
IN1A2
A2
IN
RinA2
OUTA2
R1
Rterm
Zline/2
OUT
Vin
OUTA2'
Rterm'
OUT'
IN2A2'
A2'
IN'
RinA2'
IN1A2'
R1'
Zline/2
RFA2'
RFA3'
IN1A3'
RinA3'
A3'
OUTA3'
IN2A3'
RjA3'
RFABT'
ABT'
OAA'

Fig. 2

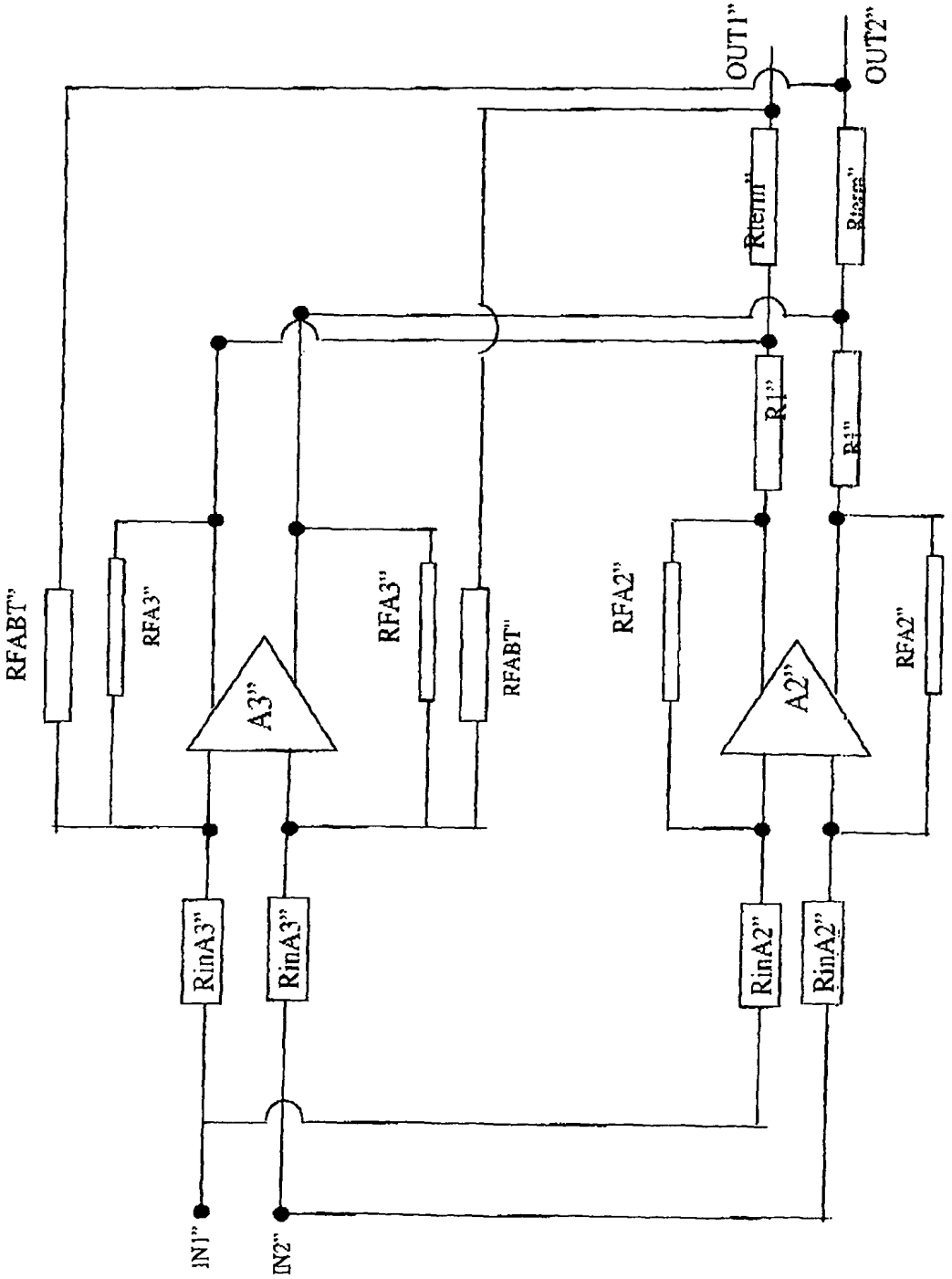
OUT1"
OUT2"
Rterm"
Rterm"
R1"
R1"
OAA"
RFABT"
RFA3"
A3"
RFA3"
RFABT"
RFA2"
A2"
RFA2"
RinA3"
RinA3"
RinA2"
RinA2"
IN1"
IN2"

Fig. 3

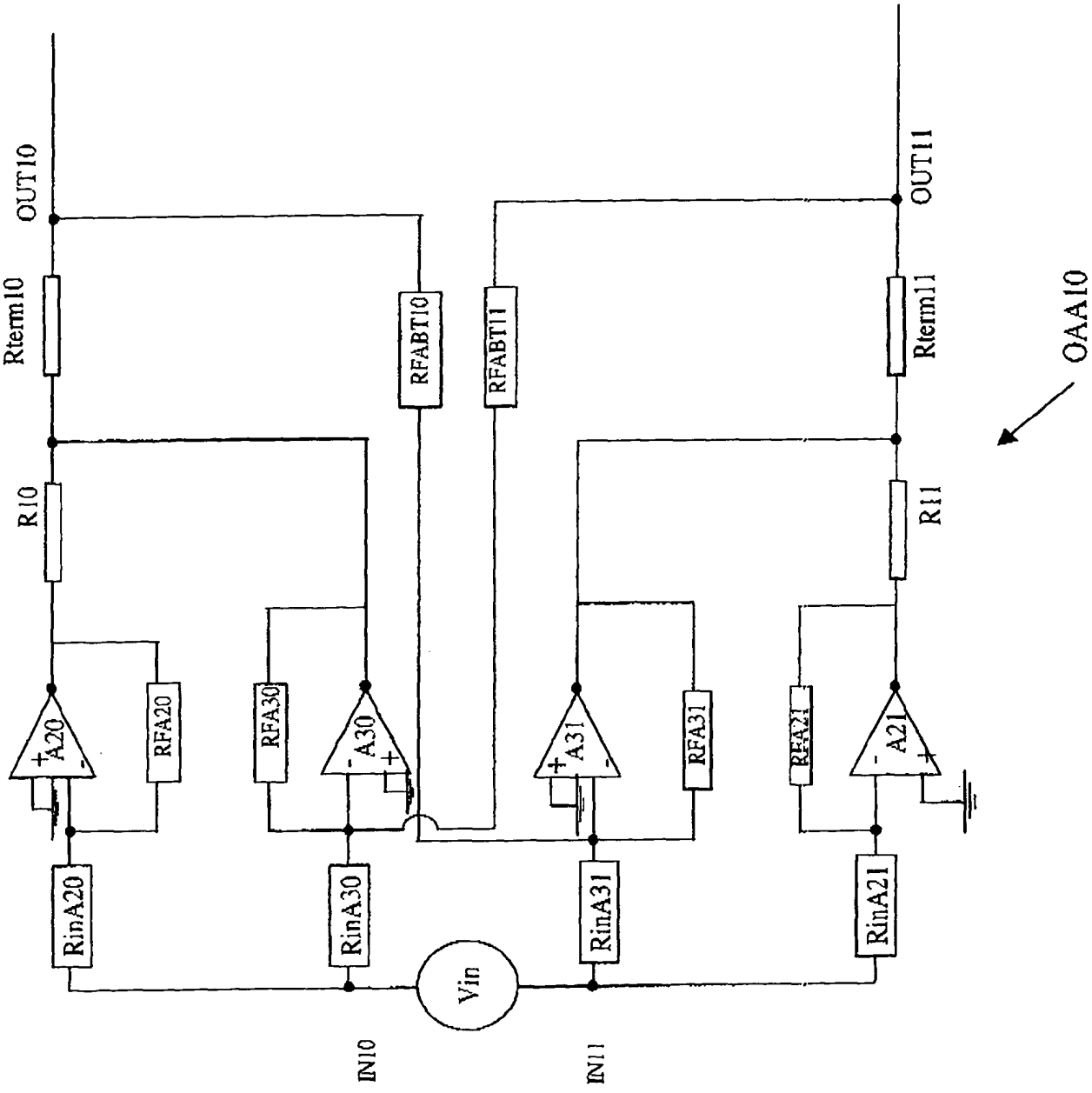
OUT10
OUT11
Rterm10
Rterm11
R10
R11
RFABT10
RFABT11
OAA10
A20
A30
A31
A21
RFA20
RFA30
RFA31
RFA21
RinA20
RinA30
RinA31
RinA21
Vin
IN10
IN11

Fig. 4

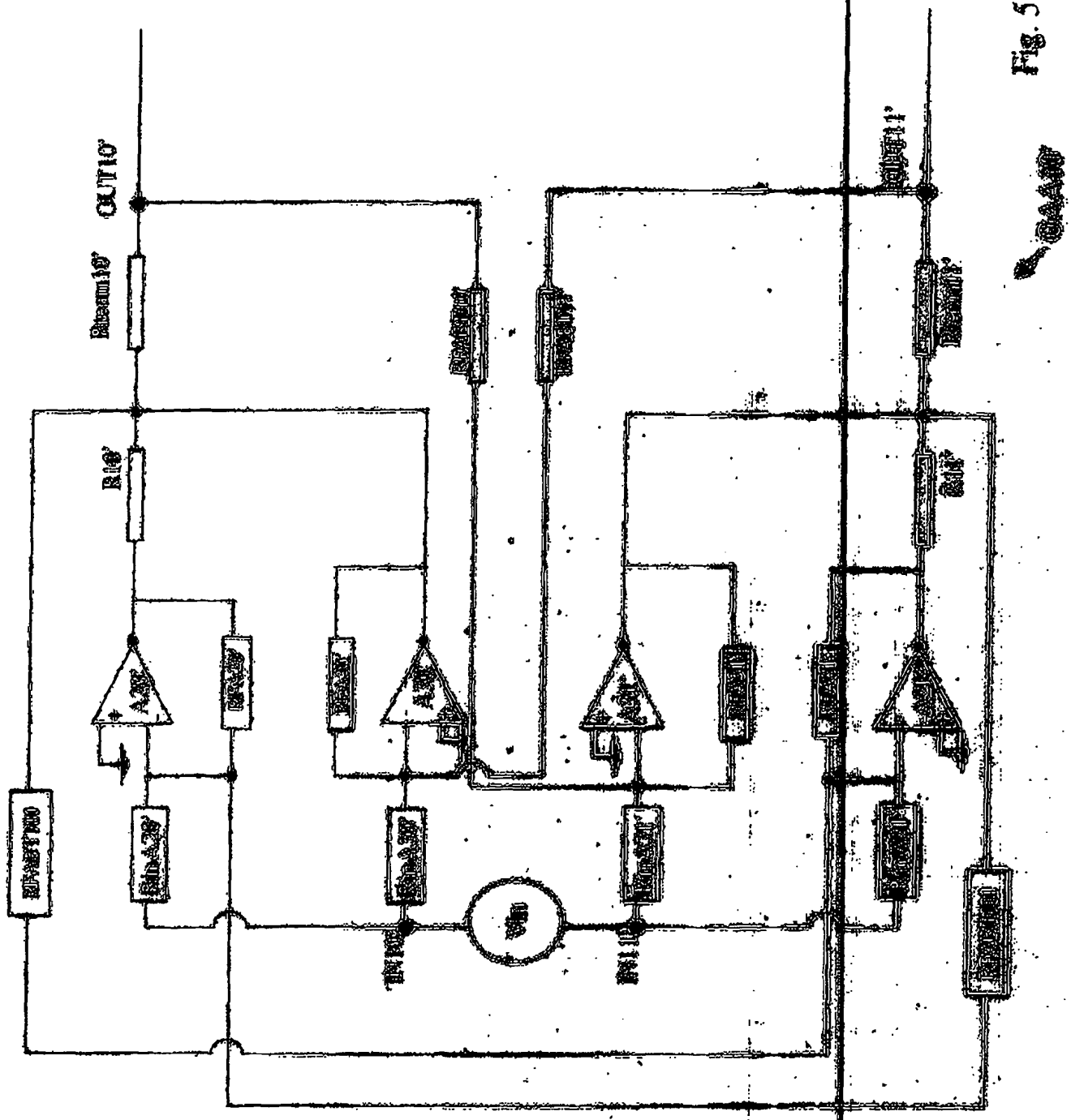

Fig. 5

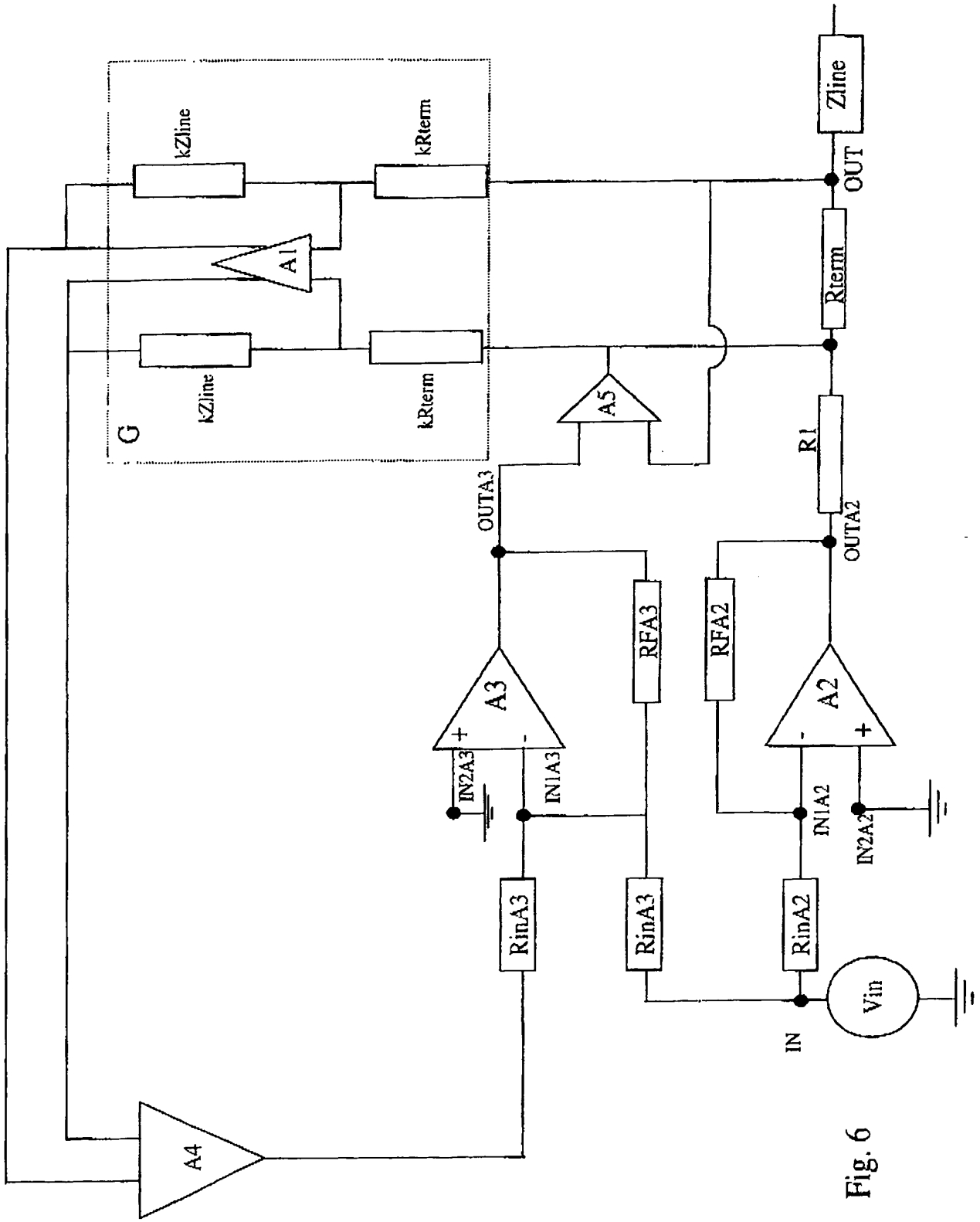
Zline
OUT
Rterm
R1
OUTA2
OUTA3
G
kZline
kRterm
kZline
kRterm
A1
A5
A4
A3
A2
RFA3
RFA2
IN2A3
IN1A3
IN1A2
IN2A2
RinA3
RinA3
RinA2
Vin
IN

Fig. 6